Sunday, April 27, 2014 - Teradyne Users Group

4:00-6:00 p.m.	Conference Check-In / Welcome Reception

Monday, April 28, 2014 - Teradyne Users Group

7:30-8:30 a.m.	**Breakfast**					
8:30-9:00 a.m.	**Welcome**					
9:00-10:00 a.m.	**Keynote Address**					
10:00-10:30 a.m.	**Break**					
10:30 a.m.–12:00 p.m.	**TEST INFRASTRUCTURE AND PRODUCTION**	**MIXED SIGNAL**	**RF WIRELESS**	**DIGITAL**	**POWER MANAGEMENT AND AUTOMOTIVE**	**ILO TRAINING**
10:30-11:00 a.m.	**IG-Link: Stop Merging and Start Linking -** *Roy Chorev & Mike Patnode Teradyne; Michael Back, Qualcomm* **(1)**	**Keeping All the Cores Busy – How to Multithread with IG-XL** *Stephen Hlotyak, Teradyne* **(3)**	**Dynamic Error Vector Magnitude (DEVM) Test for RF Power Amplifiers (PA) and Front-End-Modules (FEM) on the ETS-88 RF -** *Stephen Lyons, Aik-Moh Ng & Guillermo Pidal, Teradyne; Paul Chen, Aeroflex* **(19)**	**Measuring Switching Characteristics With or Without QTMU? -** *Maciej Miler, Texas Instruments; Jozef Molnar, Teradyne* **(38)**	**Need more time? Follow the fat rabbit! A Way to Spot and Eliminate Time-Wasting Code in Eagle EV & MST Test Programs -** *Ingo Wahl, Teradyne* **(96)**	**Pin Margin Tool & IG-XL V8.20.00 -** *Paul Picarski & Keith Thomas, Teradyne* **(170)**
11:00-11:30 a.m.	**IG-Diff - You changed what? -** *Roy Chorev, Holly Wang & Ying-Can Wei, Teradyne* **(2)**	**Implementing Concurrent Test on a Mixed Signal Device -** *Xiaorong Song, Freescale* **(136)**	**Reducing EVM Error Through Traditional Device Calibration and Error Correction by ESA for LTE Transceivers -** *Han-Won Jin & Dae-Sung Kim, Teradyne* **(97)**	**Tips for Successful Pattern Conversion to Eagle DPU16 -** *Chiau-Woon Yeo, Teradyne* **(12)**	**High Accuracy Wafer Level RDS(on) Measurement Techniques -** *Jack Weimer, Teradyne* **(31)**	
11:30 a.m.-12:00 p.m.	**IG-Data/IG-Review – What's in these 200 sheets anyway? -** *Krista Bertsch & Sherri Scharf, Teradyne* **(4)**	**Automated Eagle Wait Time Optimizer and Production Release Tool -** *Chakra Jamdagneya, Texas Instruments* **(8)**	**TD-SCDMA Demodulation and EVM -** *Lawrence Luce, Teradyne* **(15)**	**Managing SVM to Improve Test Time -** *Claude Hanchard, Teradyne* **(138)**	**Site Control Across Sectors with MST -** *Chuck Carline, Teradyne* **(54)**	
12:00-1:00 p.m.	**Lunch**					
1:00–3:30 p.m.	**TEST INFRASTRUCTURE AND PRODUCTION**	**MIXED SIGNAL**	**RF WIRELESS**	**DIGITAL**	**POWER MANAGEMENT AND AUTOMOTIVE**	**ILO TRAINING**
1:00-1:30 p.m.	**Test Time Analysis and Multisite Efficiency Made Easy -** *Adrian Carleton, Freescale* **(41)**	**Programming Sine and Cosine Waves Using the LMF on J750 -** *Hock Meng Tan, Teradyne* **(17)**	**Using the nWire DUT Clock to Capture Highly Unstable Device Clocked Data -** *Dan Buker, Teradyne* **(131)**	**System Level Test Using Protocol Aware ATE -** *Shawn Molavi, Broadcom* **(33)**	**Advanced APU Measurement Techniques -** *Chuck Carline, Teradyne* **(53)**	**TimeLines: An IG-XL Tool for Test Time Reduction -** *Paul Picarski, Teradyne* **(58)**
1:30-2:00 p.m.	**Automating Flow Simulation -** *Lai-Choon Chan, Teradyne* **(75)**	**Multi-Tone Generation on Eagle Test System Arb -** *John Lewis & Mike Robichaud, Teradyne* **(39)**	**What Do Higher Data Rates Mean to Cellular and Connectivity Testing? -** *Steven Fields, Teradyne* **(169)**	**Protocol Memory Display -** *Gopi Muthu & Pavan Ramakrishna, Teradyne* **(49)**	**APU-12 Best Practices -** *Kevin Baade & Hugh Jackson, Teradyne* **(154)**	

2:00-2:30 p.m.	**IG-XL Run-Time Error Processing: How Binning Is Determined for an Error -** *Hansung Kim, Teradyne* **(108)**	**Continuity Probe Solution -** *Alan Tham, Teradyne* **(73)**	**LTE-A Test Time Reduction with UltraWave 12G (Modulation / Demodulation) -** *Jong-ik Oh, Teradyne; Sung-Jong An, FCI* **(28)**	**Case Study: A Production Ready Project with Concurrent Test Flow and Massive PA Calls -** *Youshan Jin & Chunlei Li, Hisilicon; Troy Zhang, Teradyne* **(100)**	**96V Automotive Testing Using APU12: Trials and Tribulations -** *Joseph Yehle, Texas Instruments* **(42)**	
2:30-3:00 p.m.	**Integrating Automated Test Program Generation in Your Daily Workflow Saves Time -** *Nico Nebel, Bosch; Ralf Baumann, Teradyne* **(84)**	**How to Avoid Yield Loss Due to Site-to-Site Interaction Caused by Substrate Currents -** *Jakob Goossens, ON Semiconductor* **(101)**	**Get the Most Out of Those RF Ports You Have! -** *Stephen Pruitt, Teradyne* **(166)**	**Behavior of the PE Pin When Selecting Input/Output in the Pinmap -** *Byung-Woo Han, Teradyne; SukMin Lee, HANA Micron; SungBok Yun, Amkor* **(70)**	**Simple Method to Generate Transients of >30KV/us Using the SPU500 -** *Victor Lopez de Nava, Texas Instruments* **(135)**	
3:00-3:30 p.m.	**Break**					
3:30–5:00 p.m.	**TEST INFRASTRUCTURE AND PRODUCTION**	**MIXED SIGNAL**	**RF WIRELESS**	**DIGITAL**	**POWER MANAGEMENT AND AUTOMOTIVE**	**ILO TRAINING**
3:30-4:00 p.m.	**Associating High PTE and Resources Usage on ETS-800 for a Successful DIB Design -** *Claude Hanchard, Teradyne* **(133)**	**MATLAB 2 UltraFLEX: A Design Flow for Custom DSP Algorithm Development -** *Daniel Rosenthal, Teradyne* **(27)**	**LTE-A Transceiver Quad Sites Test by Daughter Board on UltraFLEX -** *Sang-Jin Choi & Dae-Sung Kim, Teradyne* **(98)**	**Tips on Using the nWire Engine to Generate Free-Running Clocks for Multisite Applications -** *Vic Li, Teradyne; Chihome Chung, TSMC* **(63)**	**SPU-112 SOA Characterization -** *Kevin Baade & Hugh Jackson, Teradyne* **(153)**	**Pin Margin Tool & IG-XL V8.20.00 -** *Paul Picarski & Keith Thomas, Teradyne* **(170)**
4:00-4:30 p.m.	**Getting the Most Out of the MST Environment: Tips & Techniques -** *Steven Katz, Teradyne* **(139)**	**Testing GainSpan's Ultra Low-Power WLAN SOC with Protocol Aware -** *Tony Armell, Teradyne* **(65)**	**Test Optimization For Dual RX RF Transceiver -** *Karthik Chellappa, Tessolve* **(25)**	**How to Use nWire PA to Implement All BIST Tests for High Speed Devices and Customize a Template for IP Reuse -** *Tian Gan, Teradyne; Huawei Zhang, Hisilicon* **(94)**	**Test Quality Improvement for Automotive Products -** *Davide Appello, STMicroelectronics; Tamas Kerekes, NplusT Semiconductor* **(91)**	
4:30-5:00 p.m.	**Dynamic Test Sequence Control in Eagle Test Systems Product Sheets -** *Richard Tuttle, Atmel* **(18)**	**Automated Printing of Test Resource Condition in Eagle Tester Without Using RAIDE -** *Sanoop Sukumaran, Texas Instruments* **(88)**	**Low Cost RF SOC Solution with J750Ex-HD+LitePoint -** *Tiger Feng, Teradyne; Jing Hu, Spreadtrum* **(24)**	**nWire PA Makes Digital Source/Capture More Efficient for Various Protocols on Smartphone Baseband IC -** *Rison Jia & Arthur Zhang, Teradyne; Xiaogang Li, Rongwen Xu & Yanfeng Zheng, RDA Microelectronics* **(50)**		
5:45-10:00 p.m.	**Teradyne Hospitality Event @ Angel Stadium**					

Tuesday, April 29, 2014 - Teradyne Users Group

7:30-8:30 a.m.	**Breakfast**						
8:30–10:00 a.m.	**TEST INFRASTRUCTURE AND PRODUCTION**	**MIXED SIGNAL**	**RF WIRELESS**	**DIGITAL**	**POWER MANAGEMENT AND AUTOMOTIVE**	**ILO TRAINING**	
8:30-8:45 a.m.	**TUG Business Meeting**						
8:45-10:00a.m.	**Semiconductor Business Meeting & Engineering Update**						
10:00-10:30 a.m.	**Break / Vendor Fair**						**VENDOR FAIR 10:00 a.m. - 5:00 p.m.**
10:30 a.m.–12:00 p.m.	**TEST INFRASTRUCTURE AND PRODUCTION**	**MEMORY**	**RF WIRELESS**	**DIGITAL**	**POWER MANAGEMENT AND AUTOMOTIVE**	**ILO TRAINING**	
10:30–11:00 a.m.	**A Study on Optimized Settling Time & Device Interface Board Application for Measuring Static Power Dissipation of the Device with Large Capacitor Applications** - *Roberto (Young-woo) Lee & Kang-Hoon Oh, Teradyne* **(80)**	**How to Implement the Capture Processor on the Nextest MPAC Option to Test a DAC** - *Grant Viehmann, Teradyne* **(23)**	**UltraWave 24: The Future of RF Test** - *Ron Burke, Teradyne* **(172)**	**My TF and ATPG Patterns Are Failing: Tips and Tricks to Debug Them** - *Francois Deun, Teradyne* **(26)**	**Terminating Toxic Test** - *Jack Weimer, Teradyne* **(32)**	**TimeLines: An IG-XL Tool for Test Time Reduction** - *Paul Picarski, Teradyne* **(58)**	
11:00a.m.-11:30 p.m.	**Resolving Encryption Issues with Teradyne's Test Program Protection Tool** - *Bruce Chang, Teradyne; Karl Liu, TSMC* **(64)**	**How to Use the Nextest Magnum DBM as a Digital Send Instrument** - *Grant Viehmann, Teradyne* **(126)**		**Synchronization of UltraPin800 and SB6G for JTAG Test of JESD High Speed Serial I/Os** - *Aparna Tata & Sri Lakshmi Tummala, Analog Devices* **(66)**			
11:30-12:00 p.m.	**100X Faster ASCII Worksheet Import in Excel** - *Glenn Carson, Freescale* **(45)**	**Testing 2304 ADCs Concurrently Using The Magnum I Plus MPAC Option Board** - *Bob Jamieson, Teradyne; Tor Urdalen, Atmel* **(51)**		**MIPI D-PHY Loopback Relays Can Be Replaced w/UltraFLEX UltraPin1600 Passive Loopback Path** - *Hyoung-mo Choi, Teradyne; Young-cheol Kim, Samsung* **(89)**	**Taking Full Advantage of ETS-800 APEx Architecture** - *Brent Rousseau, Teradyne* **(60)**		
12:00-1:00 p.m.	**Lunch**						

1:00–3:00 p.m.	TEST INFRASTRUCTURE AND PRODUCTION	MIXED SIGNAL	RF WIRELESS	DIGITAL	POWER MANAGEMENT AND AUTOMOTIVE	ILO TRAINING
1:00-1:30 p.m.	**Visual Basic Dictionaries: Solve Your Software Interfacing Problems -** *Lauren Guajardo, Teradyne; Christopher Kuzen, Flir Commercial Systems* **(124)**	**High-speed SerDes DAC and ADC Test Solution -** *Ryan Shi, Teradyne; Leo Liu, Hisilicon* **(82)**	**Testing Wideband IQ Signals Using UltraFLEX UltraWave 12G Receiver -** *Yu-Jen Chen & Chi-Chan Cheng, Broadcom; Young-Kun Ann, Teradyne* **(44)**	**UltraSerial10G, Jitter and Eye Analysis Over the 10.7Gbps -** *Hiroyuki Komatsuzaki, Teradyne* **(47)**	**Time Measurement of Real-World Signals -** *John Wilcox, Teradyne* **(147)**	**Pin Margin Tool & IG-XL V8.20.00 -** *Paul Picarski & Keith Thomas, Teradyne* **(170)**
1:30-2:00 p.m.		**Mixed Signal ADC Testing with the UltraVI80 Instrument -** *Stephanie Draeger, Teradyne; Keith Remlinger, Test Spectrum* **(130)**	**Multisite RF Probe on the J750** *Bruck Girma, Michael Marintzer, Jason Webb & Tengxiang Zhang, Silicon Labs* **(118)**	**Effect of Training Data Variations on the CDR Lock Time -** *Weng Kwong Yeo, Teradyne* **(29)**	**Challenges of Mobile PMIC Device Testing on ETS-800 with Direct Probe I/F -** *Min-Young Kim & Hyun-Su Kim, Teradyne* **(86)**	
2:00-2:30 p.m.	**Modular Programming on the J750 -** *Maite Chatskis & Peter Tran, Teradyne* **(119)**	**Rotating Gravity - Frequency Domain Test for MEMS -** *Dan Thornton, Analog Devices* **(145)**	**RF Performance in Array Structures Based On Ground Placement -** *Sarosh Patel & Jeff Sherry, Johnstech International* **(121)**	**High Speed and Multi-Lane Testing Using XD Module -** *Atsuko Hatta, & Hiroyuki Komatsuzaki, Teradyne* **(46)**	**Best Practices and Test Techniques with UPU-64 on ETS-800 -** *Bethany Van Wagenen, Teradyne* **(146)**	
2:30-3:00 p.m.	**Leveraging a Code Library to Speed Inter-Platform Code Application -** *Stephanie Draeger, Teradyne; Keith Remlinger, Test Spectrum* **(129)**		**Testing RFIC Devices Over DigRF v4 -** *Moris Shakeri, Broadcom; Fady Bishay, Ron Burke, Wade Shih & Shawn Sullivan, Teradyne* **(168)**			
3:00 - 5:00 pm	**VENDOR FAIR / ROUNDTABLES / POSTER SESSIONS**					
	Increasing Tester Resource Utilization Efficiency for Continuity Test to Reduce Test Time and System Resources - *Hoijik (Jimmy) Kim, FCI; Roberto Lee & Kang-Hoon Oh, Teradyne* **(95)**	**Adaptive ETS Resources Application -** *Min-Young Kim, Teradyne* **(106)**		**High Speed Digital Programming Techniques by Differential Measurement -** *Nichle Su, Teradyne* **(36)**		**TimeLines: An IG-XL Tool for Test Time Reduction -** *Paul Picarski, Teradyne* **(58)**
	High Site Count Test Solution Using 10K Probe Tower - *Daniel Park, Teradyne* **(13)**					
	PCB Integrated Solution for IC Testing - *Henry Chang, Teradyne* **(59)**					
	Examining the Throughput Benefits of Distributed vs. Centralized Multicore Computing - *Roy Chorev & Shreekar Diwakarla, Teradyne* **(109)**					

Wednesday, April 30, 2014 - Teradyne Users Group

7:30-8:30 a.m.	**Breakfast**					
8:30–10:00 a.m.	**TEST INFRASTRUCTURE AND PRODUCTION**	**MIXED SIGNAL**	**RF WIRELESS**	**DIGITAL**	**POWER MANAGEMENT AND AUTOMOTIVE**	**MEMORY**
8:30-10:00 a.m.	**Panel Discussion: Imagine the Future of Test (174)**					
10:00-10:30 a.m.	**Break**					
10:30 a.m.–12:00 p.m.	**TEST INFRASTRUCTURE AND PRODUCTION**	**MIXED SIGNAL**	**RF WIRELESS**	**DIGITAL**	**POWER MANAGEMENT AND AUTOMOTIVE**	**MEMORY**
10:30–11:00 a.m.	**Getting a Head-Start on Converting IG-XL Programs into ETS-800 MST Programs -** *Steven Katz, Teradyne* **(140)**	**HDCTO vs. MSO – Emerging Competition in the AC / Mixed Signal League -** *Rainer Gruber, Teradyne* **(102)**	**Measuring Noise Figure for RF Receivers Using UltraFLEX UltraWave 12G Receiver -** *Yu-Jen Chen & Chi-Chan Cheng, Broadcom; Young-Kun Ann, Teradyne* **(43)**	**Implementing Sflash Protocol Aware Characterization -** *Hank (Hyunkue) Kang, Broadcom; Vivian Wang, Teradyne* **(132)**	**PVI for Power/Automotive Testing: Optimizing Test for Production Environment -** *How Chuin Yoong, Teradyne; Chee Kian Chong, Infineon* **(16)**	**Memory Testing on IP750 Using Image Processing -** *Masataka Tsuji, Teradyne* **(151)**
11:00-11:30 a.m.	**New Instrument Customer Evaluation (NICE) Flow -** *Charles Esteves, Teradyne; Sundeep Desai, Texas Instruments* **(62)**	**DC Trend Removal by DSP-based Analysis on DAC Testing -** *Shawn Peng, Teradyne* **(57)**	**SerDes Testing Beyond 15GBps -** *Rien Looijen & Rien Van Oort, Salland Engineering* **(30)**	**Using DSIO to Measure Frequency on J750 -** *Kevin Giltner, Teradyne* **(137)**	**High-Voltage Detect Tool to Avoid HSD Gripen Circuit Damage -** *Alec (Chia-Min) Lin, Teradyne* **(10)**	**Using TEC Save to Find a Data Valid Window During Synchronous Tests -** *Nathan Linquist, Micron; Randal Clark, Michael Naron & Lyle Tarbet, Teradyne* **(125)**
11:30 a.m. - 12:00 p.m.	**Online Stability Study Tool -** *Miroslav Stuchlik & Jakub Tiller, ON Semiconductor* **(79)**	**Encoding and Decoding a Sine Signal for PCS 10base-G 64b66b Standard -** *Pritish Agarwal, Marc Hutner & Steve Lyons, Teradyne* **(71)**	**Probe Card Design Guidelines for Test Concurrency on RF Connectivity Devices -** *Manikandan Palanisamy, Teradyne* **(37)**	**Rise/Fall Time Measurements on J750Ex-HD -** *Lauren Guajardo & Chien Min Hwong, Teradyne* **(112)**	**Test Time Reduction: Our Story -** *Raymond Seah, Teradyne; Pan Hu, Qualcomm* **(115)**	**Massively Parallel Parametric Go/No Go Tests with Measured Results Sampling -** *Randal Clark & Larry Hatton, Teradyne* **(111)**
12:00-1:00 p.m.	**LUNCH**					

1:00–3:30 p.m.	TEST INFRASTRUCTURE AND PRODUCTION	DIGITAL	RF WIRELESS	DIGITAL	POWER MANAGEMENT AND AUTOMOTIVE	MEMORY
1:00-1:30 p.m.	**Probe Card Supernova! Best Practices and Lessons Learned to Avoid Burnt Needles -** *David Lam, Teradyne; Sundeep Desai, Texas Instruments* **(67)**	**Analytical Approach to Loadboard Design -** *Noel Del Rio, Freescale; Don Thompson& Thomas P Warwick, RD Circuits* **(141)**	**ESA Programming Overview & Test Time Reduction Methods -** *Steven Fields, Teradyne* **(173)**	**How to Optimize High Parallel Digital Test Programs -** *Ralf Baumann, Teradyne* **(105)**	**Testing Power Modules and Smart Power Modules with the ETS-2500 -** *Hector Valdez, Teradyne* **(68)**	**KGD Memory Testing at 2.133Gbps -** *Wade Bick, Craig DiPalo, Leebo Shim, Luis Valiente & Vlad Vayner, Teradyne* **(117)**
1:30-2:00 p.m.	**ETS-364 Eagle Vision/ETS-88-MST/ETS-800-MST Upgrade Process for Windows 7 Offline Systems -** *Lam Tran, Texas Instruments* **(5)**	**Signal Integrity -** *Teppei Yamaguchi, Teradyne* **(150)**		**Speeding up Test Programs for High Site Counts on J750Ex-HD -** *Leo Di Bello, Teradyne* **(120)**	**Understanding Index Parallel Testing -** *Ed Mateyka, Teradyne* **(144)**	**Advanced Shmoo Features on Magnum -** *Brendan Ryan, Teradyne* **(116)**
2:00-2:30 p.m.		**Testing High Current Switch Devices with Ganging 10 HexVS Supplies -** *Richard Matte, Broadcom; Vivian Wang, Teradyne* **(143)**		**The Benefits and Use Model for Concurrent Pattern Testing on the J750Ex-HD -** *Daniel Murphy, Teradyne* **(127)**		**Controlling Voltages in a Pattern on the Nextest Magnum I -** *Brandon Bohlen & Patrick O'Connell, Cypress Semiconductor* **(152)**
2:30-3:00 p.m.		**Comparing UltraPin1600 HRAM, CMEM and DSSC Digital Capture -** *Pritish Agarwal & Ann Yong, Teradyne* **(72)**	**Effect of DC Supplies on RF Transient Response -** *Keith Carroll & Patty Carroll, Teradyne* **(171)**	**Application of Auto Strobe and DIB Access in J750Ex-HD -** *Haohui Gu, Teradyne* **(74)**		**Even Parity Subroutines Are Reusable for Your Embedded ARM! -** *Ross Youngblood, Teradyne* **(122)**
3:00-3:30 p.m.						**Building Your Own Tester GUI For The ARM Debug Access Port -** *Ross Youngblood, Teradyne* **(123)**
3:30 - 5:30 p.m.	Survivor Party					