

# HOT TOPICS

## DEFENSE & AEROSPACE

- Boundary Scan
- ATLAS Integration
- Characterization of Legacy ATS for Replacing Instruments that do not have a Compatible COTS Replacement
- Mixed Signal Testing with the Ai-760 and the Di-Series
- Parallel/Operational Test with the Ai-7 Series
- Testing Unique Busses Using the Bi4-Series and HSSub
- Sending and Receiving Data with the Di-Series
- Spectrum 9100-Series M9-Series to Di-Series Migration
- Techniques for New Di-Series TPS Development
- Enhancing Existing Tests with New Instrument capabilities
- System Characterization for Instrument Replacement

## DIGITAL

- Using Protocol Aware for Speed or Simplicity
- Device Jitter Measurement Techniques
- DIB Design Techniques for Gigabit-per-second
- Digital Signals
- Memory Test Improvements
- High-speed Serial Interface Testing
- Highly Parallel Test
- Concurrent Test: Using Multiple Time Domains and Protocol Aware Engines
- New Techniques for Reducing Cost of Test

## MIXED SIGNAL

- Best Techniques for the DSSC - DigSrc and DigCap
- Concurrent Test Implementations and Tools
- Digital Signal Processing Algorithms and Techniques
- Low-leakage DIB Design Techniques
- Overcoming the Challenges Encountered in the Testing of MEMS Devices
- Parallel Test Efficiency
- Techniques for Optimizing Test Program Throughput

## POWER MANAGEMENT/AUTOMOTIVE

- DIB Design Techniques for Automotive Devices
- New Emerging Markets in Automotive
- SMPS Test Techniques
- Techniques for Optimizing Test Program Throughput
- Test For Quality
  - Iddq Testing
  - Stress Testing

## RF WIRELESS

- RF Wafer Probe
- Wafer Level Chip Scale Package Testing of RF Devices
- Techniques for Optimizing Test Program Throughput
- Device Characterization using the UltraFLEX
- Testing LTE Devices
- Testing 802.11ac Devices
- Testing RFID's and NFC devices

## TEST INFRASTRUCTURE AND PRODUCTION

- 3D Packaging Test Strategies
- Adaptive Test Flows for Improving Throughput
- Benchmarking Tester Performance
- DUT Board Considerations For Highly Parallel Test
- Reduced Pin Count Test
- Software Tools for Improved Test Development Productivity
- Test Program Architecture to Facilitate Code Reuse and Program Modularity
- Testing with Strip Handlers: Lessons Learned and Benefits Gained
- Yield Learning and Diagnostics