HOT TOPICS

DEFENSE & AEROSPACE

- ATLAS Integration
- Characterization of Legacy ATS for replacing instruments that do not have a compatible COTS replacement
- Windows XP to Windows 7/8 Migration
- Testing unique busses using the HSSub
- Spectrum 9100-Series M9-Series to Di-Series Migration
- Techniques for new Di-Series TPS Development
- Tester Replaceable Unit Obsolescence Management and Replacement

DIGITAL

- Concurrent Test: Using Multiple Time Domains and Protocol Aware Engines
- Eye and Jitter Measurement Techniques
- Memory Test Improvements
- Using Protocol Aware for Speed or Simplicity
- High-speed Serial Interface Testing
- Analyzing Pattern Failure Data
- New Techniques for Reducing Cost of Test

MEMORY

- Concurrent Test of Multi-chip Devices
- High-speed Memory Test Techniques
- Memory BIST Test Techniques
- Mixed Memory-Logic Testing
- Reduced Pin Count Device Testing
- DIB Design Considerations for High-speed and Multi-chip Devices

MIXED SIGNAL

- Best techniques for the DSSC - DigSrc and DigCap
- Digital Signal Processing Algorithms and Techniques
- Parallel Test Efficiency
- Techniques for Optimizing Test Program Throughput

POWER MANAGEMENT/AUTOMOTIVE

- Auto "Infotainment" System added test restrictions / requirements for PMIC
- Techniques and Best Practices for creating Modular PMIC code, not as easy as you think!
- Optimizing Eagle test platforms (ETS364, ETS88, ETS800) and instruments for Automotive and PMIC test
- Hardware Design Consideration for Automotive Devices
- Simplifying load boards.... or not
- High voltage/current probe, preventing probe damage
- Instrument sharing methodology
- SMPS Test Techniques: Build the ‘system or test the silicon?
- Techniques for optimizing test program throughput
- New emerging markets in Automotive Integrated sensor test (temperature, pressure)

RF WIRELESS

- Low Cost RF Platforms
- Testing LTE Devices
- 802.11ad and Automotive Radar (60+ GHz)Wafer level chip scale package testing of RF devices
- Device Characterization using the UltraFLEX
- Testing 802.11ac Devices
- Testing RFID's and NFC devices

TEST INFRASTRUCTURE AND PRODUCTION

- Test Program Meta-Language and Automatic Test Code Generation
- Sophisticated Automation of ATE Systems
- Adaptive Test Flows for Improving Throughput
- Benchmarking Tester Performance
- DUT Board Considerations For Highly Parallel Test
- Software Tools for Improved Test Development Productivity
- Test Program Architecture to Facilitate Code Reuse and Program Modularity
- Testing with Strip Handlers: Lessons Learned and Benefits Gained
- Yield Learning and Diagnostics
- Preventing Electrical Over-Stress (EOS) conditions

FOR MORE INFORMATION, VISIT WWW.TERADYNE.COM/TUG

TUG 2015
TERADYNE USERS GROUP
MAY 4-6 · ORLANDO, FLORIDA · EXPLORE THE UNIVERSE OF TEST